IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Lines et al.

Application No.: 10/667,152

Filed: September 16, 2003

Title: ASYNCHRONOUS MULTIPLE-ORDER
ISSUE SYSTEM ARCHITECTURE

Attorney Docket No.: FULCP006

Examiner: Not yet assigned

Group: 2183

INFORMATION DISCLOSURE STATEMENT
37 CFR §§1.56 AND 1.97(b)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The references listed in the attached PTO Form 1449, copies of which are attached, may be material to examination of the above-identified patent application. Applicants submit these references in compliance with their duty of disclosure pursuant to 37 CFR §§1.56 and 1.97. The Examiner is requested to make these references of official record in this application.
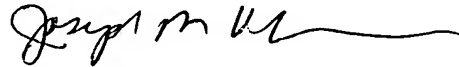
This Information Disclosure Statement is not to be construed as a representation that a search has been made, that additional information material to the examination of this application does not exist, or that these references indeed constitute prior art.

This Information Disclosure Statement is: (i) filed within three (3) months of the filing date of the above-referenced application, (ii) believed to be filed before the mailing date of a first Office Action on the merits, or (iii) believed to be filed before the mailing of a first Office Action after the filing of a Request for Continued Examination under §1.114. Accordingly, it is believed that no fees are due in connection with the filing of this Information Disclosure

Statement. However, if it is determined that any fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 500388 (Order No. FULCP006).
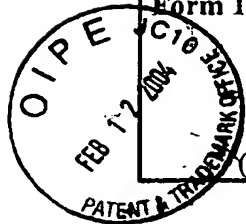
Respectfully submitted,

BEYER WEAVER & THOMAS, LLP

Joseph M. Villeneuve
Registration No.

P.O. Box 778
Berkeley, CA 94704-0778

Form 1449 (Modified) **Information Disclosure Statement By Applicant** (Use Several Sheets if Necessary)	Atty Docket No. FULCP006 Applicant: Lines et al. Filing Date September 16, 2003	Application No.: 10/667,152 Group 2183

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A1	6,038,656	03.14.00	Martin et al.			
	A2	5,752,070	05.12.98	Martin et al.			
	A3	6,044,061	03.28.00	Aybay et al.			
	A4	5,832,303	11.03.98	Murase et al.			
	A5	6,230,228	05.08.01	Eskandari et al.			
	A6	5,802,055	09.01.98	Krein et al.			
	A7	6,279,065	08.21.01	Chin et al.			
	A8	6,301,630	10.09.01	Chen et al.			

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	C1	Andrew Matthew Lines, Pipelined Asynchronous Circuits, June 1995, revised June 1998, pp. 1-37.
	C2	Alain J. Martin, Compiling Communicating Processes into Delay-Insensitive VLSI Circuits, December 31, 1985, Department of Computer Science California Institute of Technology, Pasadena, California, pp. 1-16.
	C3	Alain J. Martin, Erratum: Synthesis of Asynchronous VLSI Circuits, March 22, 2000, Department of Computer Science California Institute of Technology, Pasadena, California, pp. 1-143.
	C4	U.V. Cummings, et al. An Asynchronous Pipelined Lattice Structure Filter, Department of Computer Science California Institute of Technology, Pasadena, California, pp. 1-8.
	C5	Alain J. Martin, et al. The Design of an Asynchronous MIPS R3000 Microprocessor, Department of Computer Science California Institute of Technology, Pasadena, California, pp. 1-18.
	C6	U.S. Application 09/501,638, filed on February 10, 2000, entitled, "Reshuffled Communications Processes in Pipelined Asynchronous Circuits".
	C7	Lee et al., "Crossbar-Based Gigabit Packet Switch with an Input-Polling Shared Bus Arbitration Mechanism", September 21, 1997, XVI World Telecom Congress Proceedings, Interactive Session 3 – Systems Technology & Engineering, pp. 435-441.
	C8	Ghosh et al., "Distributed Control Schemes for Fast Arbitration in Large Crossbar Networks", March 1994, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 2, No. 1, pp. 55-67.
Examiner		Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.